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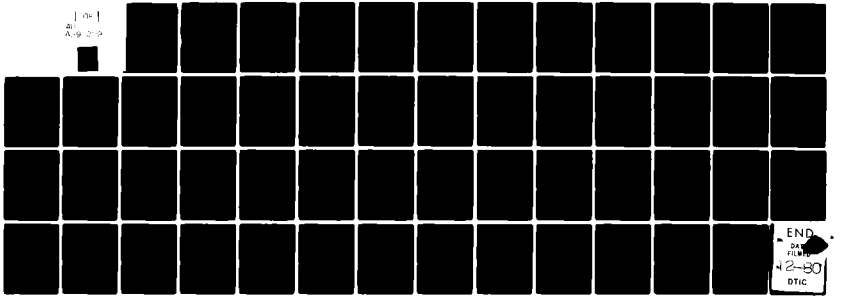

RESEARCH AND DEVELOPMENT TECHNICAL REPORT

PROCESS VARIABLE DEPENDENCE AND INTERRELATIONSHIP BETWEEN AVALANCHE INJECTED AND RADIATION INDUCED CARRIER TRAPPING IN THERMAL OXIDES

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Characterization of the process dependence of avalance injected electrons and holes in thermally grown silicon dioxide has been carried out. Process parameters investigated include oxidation temperature (900°, 1000°, and 1100°C), oxidation ambient (O_2, H_2O, and O_2/HCl), post-oxidation in situ anneal ambient (N_2, Ar), cooling ambient (O_2, N_2, Ar, and H_2O), cooling rates (<3 sec, 2 min, and 10 min), and post-metallization anneal ambients (N_2, N_2/H_2). Results

indicate basic differences between the process dependence of electron traps and that of hole traps while excellent agreement is obtained between avalanche injected and radiation induced hole trapping. Characteristics of the process dependence of hole traps are: a minimum for dry O_2 oxides, an increase for N_2 post oxidation anneals a 1000°C and above, and a high density for HCl/O_2 and steam grown oxides. Electron trap densities are minimum at 1100°C and highest for steam grown oxides although post oxidation anneals at 1000°C are effective in their reduction. Post-metallization anneal ambients were found to have little or no effect on the measured trapping of both holes and electrons.

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PURPOSE

The primary objective of this program is the investigation of the effects of processing vairables on the trapping characteristics of injected charge carriers in thermal silicon dioxide. In addition, the nature and process dependence of these trapped charges will be compared to those produced by ionizing radiation in oxides prepared simultaneously. The results obtained from this program should help in the determination of optimum process conditions for minimizing hot carrier trapping in VLSI device structures and in the establishment of accelerated test procedures for the evaluation of radiation trapping properties of thermal oxides.

TABLE OF CONTENTS

SECTION		PAGE
1.0	INTRODUCTION	1
2.0	BACKGROUND	2
3.0	EXPERIMENTAL PROCEDURE	7
4.0	RESULTS AND DISCUSSION	12
5.0	SUMMARY AND CONCLUSIONS	38
	ACKNOWLEDGMENTS	40
	REFERENCES	41

LIST OF ILLUSTRATIONS

FIGURE		PAGE
2-1	The four types of charges associated with the thermally oxidized silicon structure.	3
3-1	Schematic diagram of the automated avalanche injection and trapping system.	10
4-1	Fixed oxide charge (N_f) versus oxidation temperature for n- and p-type (111) silicon wafers oxidized in dry O_2 and annealed/cooled in O_2, N_2, and Ar (N_2, Ar anneal time = 10 min). Oxide thickness x_o = 790-860 Å and post-metallization anneal (PMA) = 400°C/10% H_2 in N_2/10 min.	15
4-2	Typical output from the automated avalanche carrier injection and trapping system.	16
4-3	Flat band voltage shift versus injection time for hole trapping from n-type (111) silicon oxidized in dry O_2 at 1000°C. Current density J = 4.5 x 10^{-8} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.	18
4-4	Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in dry O_2 and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 4.5 x 10^{-8} A/cm^2.	19
4-5	ℓn d/dt (V_{FB}) versus time for a sample oxidized in dry O_2 at 1000°C. The sample received an in situ anneal in nitrogen for 10 min and was cooled in N_2. The post metallization anneal treatment was: 400°C, 10% H_2 in N_2, 10 min. Current density J = 4.5 x 10^{-8} A/cm^2.	22

FIGURE		PAGE
4-6	Change in inversion voltage following irradiation versus oxidation temperature for hole trapping from n-type (111) substrates. Samples were oxidized in dry O_2 and received a post-metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Irradiation parameters: 10^6 Rads, +10 V.	24
4-7	Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (111) substrates. Samples were oxidized in dry O_2 and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 1.5×10^{-5} A/cm^2.	25
4-8	Effective fixed oxide charge density (N_f) and interface trapped charge density (D_{it}) versus electron avalanche injection time. Samples were oxidized in dry O_2 at 900°C and cooled slowly in oxygen (O_2 SP).	27
4-9	Flat band voltage shift versus injection time for hole trapping from n-type (111) silicon oxidized in pyrogenic steam at 1000°C. Current density J = 4.5×10^{-8} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.	31
4-10	Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in steam and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 4.5×10^{-8} A/cm^2.	32
4-11	Flat band voltage shift versus injection time for electron trapping from p-type (111) silicon oxidized in pyrogenic steam at 1000°C. Current density J = 1.5×10^{-5} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.	33

FIGURE		PAGE
4-12	Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (111) substrates. Samples were oxidized in steam and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density = J 1.5×10^{-5} A/cm^2.	35

LIST OF TABLES

TABLE		PAGE
3-1	Summary of Process Conditions Employed in Experiments Dealing with Avalanche Injected and Radiation Induced Trapped Charge	9
4-1	Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for N-Type (111) Silicon Wafers Oxidized in Dry O_2	13
4-2	Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for P-Type (111) Silicon Wafers Oxidized in Dry Oxygen	14
4-3	Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for N-Type (111) Silicon Wafers Oxidized in Steam	28
4-4	Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for P-Type (111) Silicon Wafers Oxidized in Steam	29
4-5	Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for P- and N-Type (111) Silicon Wafers Oxidized in 5% HCl/O_2 at 1000°C	36

1.0 INTRODUCTION

A joint program has been established between Fairchild and the Naval Research Laboratories, the purpose of which is to characterize the process dependence of injected electrons and holes in thermally grown silicon oxides. The nature of the trapped charge is compared with those produced by ionizing radiation in oxides prepared under similar conditions. Results from this program should permit the optimization of the process conditions necessary for VLSI device structures with minimum hot carrier trapping.

MOS test capacitor structures have been prepared at Fairchild under controlled conditions. Process parameters under investigation include oxidation ambient (O_2, H_2O, and O_2/HCl), cooling ambient (O_2, N_2, and Ar), post-oxidation in situ anneal (N_2, Ar), and post-metallization anneals (N_2, N_2/H_2). Carrier injection has been achieved by avalanche from a doped substrate (10^{16}-$10^{17}/cm^3$). The change in flat band voltage as a function of injection time (for a constant injection current) was monitored through a computerized system. Quasistatic C-V measurement coupled with high frequency measurements have been used to observe interface state generation during the injection process.

MOS structures were also sent to the Naval Research Laboratory where they were subjected to ionizing radiation. Induced charges have been examined in order to correlate the results with the avalanche trapping data.

2.0 BACKGROUND

Thermal silicon dioxide has played a key role in the development and growth of the semiconductor industry. Thermally grown silicon dioxide layers have been used for many circuit functions (1) including surface passivation, insulation between layers of metal and/or polycrystalline silicon, and as actual circuit components, as well as for many processing functions such as masking against dopant diffusion and ion implantation.

Thermal SiO_2 layers are formed at temperatures of 700°-1200°C in dry oxygen, wet oxygen, pyrogenic steam, or mixtures thereof at 1 atm and in more recent technological developments at pressures extending up to 25 atm in commercially available systems (2). The growth kinetics of thermal silicon dioxide films have been characterized by a general relationship (3) and the electrical properties of the films are found to be intimately related to the oxidation growth parameters such as oxidation ambient, post oxidation anneals, and cooling rates.

The thermally oxidized silicon system has been characterized by four types of charges (4). These charges are indciated in the cross section of Fig. 2-1 and are:*

N_f - fixed oxide charge, located in the oxide near the $Si-SiO_2$ interface

N_{it} / D_{it} - interface trapped charge or states, located at the $Si-SiO_2$ interface and in electrical communication with the silicon

---

*$N \equiv Q/q$ is the effective number of charges at the $Si-SiO_2$ interface in units of cm^{-2}.

$D_{it} \equiv$ density of interface trapped charge at the $Si-SiO_2$ interface in units of $cm^{-2}\text{-}eV^{-1}$.

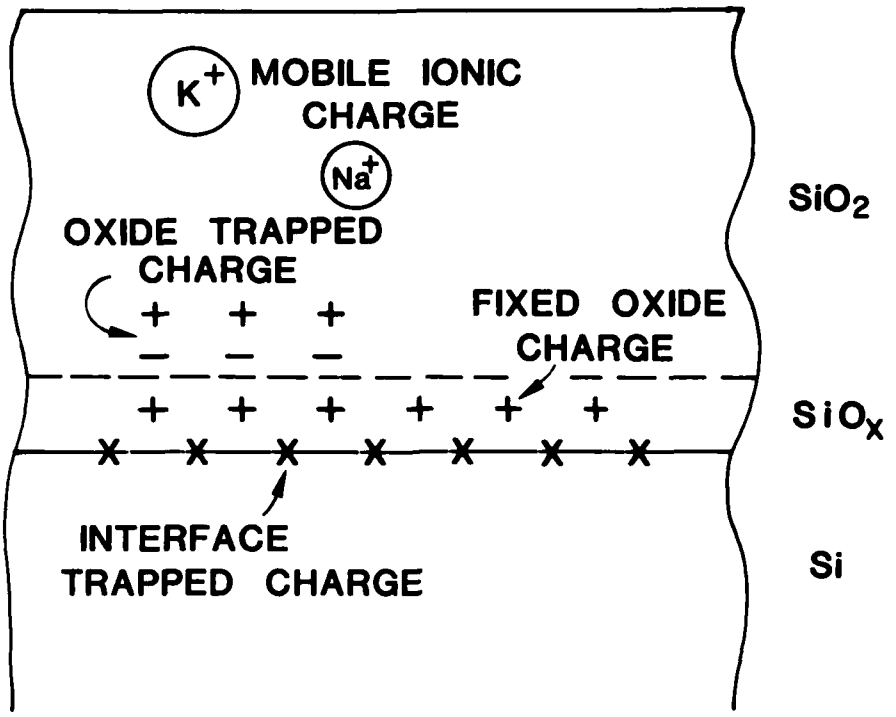

Fig. 2-1. The four types of charges associated with the thermally oxidized silicon structure.

N_m - mobile ionic charge, located throughout the oxide, and generally a positive alkali ion (Na^+, H^+)

N_{ot} - oxide trapped charge, located at the interface and/or the bulk of the SiO_2, made up of electrons or holes trapped by various means in the oxide

Of these four types of charges, N_f and N_{it} are known to be associated with the oxidation process. The oxide fixed charge has been postulated to arise from partially ionized silicon, while the structural type of interface states seem to have a similar origin, possibly trivalent silicon tied to three silicon atoms (4-6). Direct relationships between N_f and N_{it} and process variables such as silicon orientation, oxidation temperature, and annealing/cooling conditions have been investigated thoroughly (7-11) and the interdependence of N_f and N_{it} documented (11).

The oxide trapped charges, which include both trapped electrons and holes, have been investigated by various means including internal photoemission (12-14), avalanche injection of substrate by means of voltage pulses (15-17), avalanche injection by means of p-n junctions (18), optically induced hot electrons from n-channel silicon gate structures (19), forward biased p-n junctions using epitaxial silicon layers (18-20), high electric fields (21), ionizing radiation such as x-rays (22-24), γ-rays (25), VUV light (26-28), and high energy electrons (29). The considerable amount of work carried out dealing with oxide trapped charge is a reflection of the importance attached to understanding both the process dependence as well as the physical origin of the trapped charge.

The main reasons behind the increasing interest in charge trapping in thermal oxides are primarily related to device reliability, particularly in the case of MOS devices. It has been proposed that new processing techniques now being introduced such as sputtering, plasma etching and stripping, electron beam and x-ray lithography, as well as established processes such as electron beam metal evaporation and ion implantation through gate oxides (30-32) can produce neutral oxide traps. These traps could, during subsequent radiation, be a major source of device degradation. The selection of optimum process techniques is therefore becoming more critical to advanced device fabrication. Furthermore, new constraints are being imposed by device scaling in the continuing effort to achieve packing densities and better performance. Shrinking geometries can lead to increasing electric field intensities which in turn result in hot carrier generation and injection into the oxide. In present devices, sources of hot carriers such as p-n junction avalanche plasmas, channel currents, multiplication currents associated with channel currents, thermally generated leakage current, and forward bias supply currents can result in carrier injection in the oxide and subsequent trapping. This trapping can affect gain, saturation conductance, and effective threshold voltage (33). These and other adverse effects can cause degradation in both bipolar and MOS devices.

The process dependence of the oxide trapped charge resulting from radiation has been recognized for some time (34) and similarity between radiation induced hole trapping and avalanche injected hole trapping suggested in dry O_2 oxides (35). The process dependence of electron trapping for oxides grown in dry O_2 at 1000°C with different cooling procedures was investigated at 295 and 77 K (36). In this work we examine the process dependence of both electron and hole trapping by avalanche injection and the interrelationship between avalanche injection

and radiation induced charge trapping. The process parameters investigated include oxidation ambient, (dry O_2, pyrogenic steam, and O_2/HCl), post-oxidation in-situ anneal ambients (N_2,Ar), cooling ambient and rate (O_2, N_2, and Ar - <3 sec, 2, and 10 min), and post-metallization anneal ambient (N_2, N_2/H_2). The generation of interface states during avalanche injection is briefly examined in order to increase our understanding of the mechanisms involved in carrier trapping in the thermally oxidized silicon system.

3.0 EXPERIMENTAL PROCEDURE

3.1 Sample Preparation

The silicon used for the experiments was n- and p-type (111) silicon of resistivity 0.2-0.3 Ω-cm and 0.4-0.7 Ω-cm respectively. The silicon was produced at Fairchild and was in the form of 2-inch (n-type) and 3-inch (p-type) diameter wafers, chem-mechanically polished on one side and etched on the other side. The samples were cleaned in hot sulfuric acid, aqua regia, 10:1 DI water: hydrofluoric acid, and 2-propanol vapor, with appropriate deionized water rinses. The wafers were then loaded into an oxidation furnace in the appropriate ambient, oxidized for a given time, and then pulled from the furnace either in the oxidizing ambient or in nitrogen or argon. Pull rates varied from 1-3 seconds (fast pull "FP") to 2-10 minutes (slow pull "SP").

Dry oxygen was supplied from a liquid source, as were nitrogen, hydrogen, and argon. The pyrogenic steam oxidations were carried out by the direct reaction of H_2 and O_2 in a pyrogenic system. For the HCl/O_2 oxidations, HCl of 99.99% purity was supplied from a gaseous bottle source. Calibrated flowmeters were used to monitor and control gas mixtures in the proper ratios. The oxidation systems were conventional hot wall, resistance-heated furnaces with quartz tubes and high purity mullite liners.

Following oxidation, 1 μm thick Al-Cu-Si* films were vacuum deposited on the oxides by cold flash (no substrate heating) in order to avoid radiation effects from e-beam evaporations. Metal dots approximately 750 μm in diameter were formed by photolithography. Following dot definition the oxide was

*Al-4%Cu-2%Si

removed from the back of the wafers and Al-Cu-Si deposited on the back in the manner described above.

One half of each wafer was annealed at 400°C in nitrogen for 10 minutes while the other half was annealed in 10% H_2 in N_2 also at 400°C for 10 minutes. Values of N_f and N_{it} for each wafer were determined prior to avalanche injection and wafers from each run sent to the Naval Research Laboratories for radiation evaluation.

Table 3-1 contains a summary of the process conditions used in the growth of thermal oxides during this investigation.

3.2 Charge Injection and Measurements

Charge injection was carried out by driving the MOS capacitor structures into deep depletion by means of a large ac signal. The frequency of the applied signal should be sufficient to prevent the formation of an inversion layer while its amplitude is chosen such that the field in the substrate will result in avalanche carrier multiplication. The carriers generated by the avalanche process are then accelerated by the field with the minority carriers moving towards the Si-SiO_2 interface. Some carriers arriving at the interface will have sufficient energy to surmount the field lowered potential barrier at the interface. Most of the injected carriers drift through the SiO_2 and are collected at the fieldplate. However, a percentage of these carriers are trapped in the oxide and the details of that process is of great interest as pointed out previously.

Figure 3-1 shows a schematic of the automated trapping system used. The method of injection is similar to that used successfully at IBM (35,37). The measurement is carried out by switching the samples between two circuits, a capacitance

TABLE 3-1

Summary of Process Conditions Employed in Experiments
Dealing with Avalanche Injected and Radiation Induced Trapped Charge

Run No.	Wafer Type	Oxidation Ambient	Oxidation Temp(°C)	Post-Ox Anneal Ambient*	Cooling Ambient	Pull Condition
TR1/TR21	N(111)/P(111)	Dry O_2	900	--	O_2	1-3 sec
TR2/TR22	"	"	"	--	O_2	10 min
TR3/TR23	"	"	"	N_2	N_2	2 min
TR4/TR24	"	"	"	Ar	Ar	2 min
TR5/TR17	"	"	1000	--	O_2	1-3 sec
TR6/TR18	"	"	"	--	O_2	10 min
TR7/TR19	"	"	"	N_2	N_2	2 min
TR8/TR20	"	"	"	Ar	Ar	2 min
TR9/TR13	"	"	1100	--	O_2	1-3 sec
TR10/TR14	"	"	"	--	O_2	10 min
TR11/TR15	"	"	"	N_2	N_2	2 min
TR12/TR16	"	"	"	Ar	Ar	2 min
TR25/TR40	"	H_2O	900	--	H_2O	1-3 sec
TR26/TR41	"	"	"	N_2	N_2	2 min
TR27/TR42	"	"	"	Ar	Ar	2 min
TR28/TR37	"	"	1000	--	H_2O	1-3 sec
TR29/TR38	"	"	"	N_2	N_2	2 min
TR30/TR39	"	"	"	Ar	Ar	2 min
TR31/TR34	"	"	1100	--	H_2O	1-3 sec
TR32/TR35	"	"	"	N_2	N_2	2 min
TR33/TR36	"	"	"	Ar	Ar	2 min
TR43/TR45	"	O_2/HCl	1000	Ar	Ar	2 min
TR44/TR46	"	"	"	N_2	N_2	2 min

* Anneal is in situ for 10 minutes

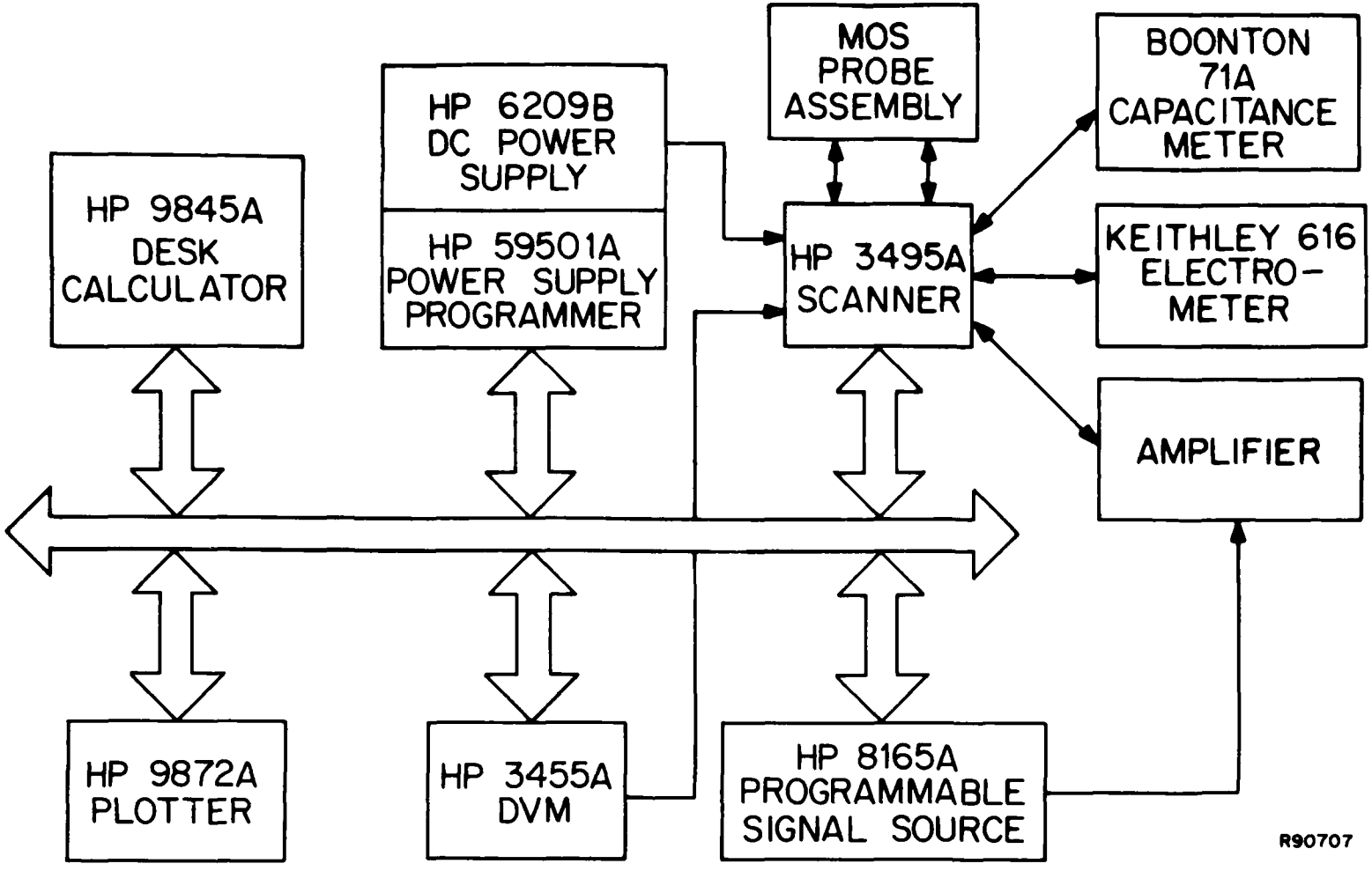

Fig. 3-1. Schematic diagram of the automated avalanche injection and trapping system.

measuring circuit and an avalanche injection circuit. The MOS structure is first switched to the C-V circuit and a 1 MHz curve obtained on the virgin capacitor. The capacitor is then switched automatically by the calculator/controller to the injection circuit where an ac signal of predetermined amplitude and frequency is applied. The current flow is monitored by a Keithly 616 electrometer and the value of current kept constant by adjusting the amplitude of the ac signal every 1/3 second. All operations and data gathering are carried out by the calculator/controller through an HP-IB bus. Flat band voltage changes resulting from the avalanche injection are obtained by switching back to the C-V circuit every 70 sec. Plots of changes in V_{FB} and in $d/dt(V_{FB})$ versus time are generated and a capture cross section and effective density of traps can be calculated from a trap model where the probability of trapping is proportional to the number of unfilled traps (19).

It should be noted that although flat band voltage shift (ΔV_{FB}) are used exclusively in the data reported here, interface state density increases can result in threshold voltage changes (ΔV_{TH}) which exceed the change in the flat band voltage. In some cases a decrease in V_{FB} is accompanied by an increase in V_{TH} as it would be in the case of simultaneous electron trapping and generation of donor-like interface states.

4.0 RESULTS AND DISCUSSION

4.1 Trapping in Dry O_2 Oxides

N- and p-type (111) silicon wafers with run numbers TR-1 through TR-24 were oxidized in dry O_2 at 900°, 1000°, and 1100°C. Table 3-1 includes the detailed processing of the samples including post-oxidation anneals and cooling conditions. More information about these wafers, including initial levels of fixed oxide charge and interface trap densities are included in Tables 4-1 and 4-2. The data represent the average of three or more capacitors scattered across the wafer. Figure 4-1 summarizes the fixed oxide charge data for both n- and p-type wafers, which indicate that:

(a) slow pull in oxygen results in the highest level of fixed oxide charge,

(b) nitrogen or argon slow pulls yield the lowest levels of charges at these temperatures (longer N_2 or Ar anneal times at 900° and 1000°C will reduce fixed oxide charge density further),

(c) the oxygen triangle effect or "N_f-O_2" triangle (7,11,38) can be observed from the oxygen fast pull data.

Once the basic data about oxide charges (N_f and N_{it}) have been gathered for each wafer the avalanche trapping experiments are carried out. A typical output from the system (Fig. 4-2) shows the initial C-V trace at 1 MHz, the final C-V trace following more than 4,000 sec of injection time and the flat band voltage shift as a function of time.

4.1.1 Hole Trapping in Dry O_2

For purposes of summarizing the data obtained in a clear manner and in order to highlight those processes resulting in a minimum flat band voltage shift, all oxides tested were approximately 800 Å thick, with a capacitor area $\simeq 4.5 \times 10^{-3}$ cm^2.

TABLE 4-1

Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) For N-Type (111) Silicon Wafers Oxidized in Dry O_2

Run No.	Oxidation Temp (°C)	Ox/ Anneal Ambient	Ox/ Anneal/Cool Time*(min)	Cool Condition**	Oxide Thickness (μm)	$N_f(10^{11}/cm^2)$†		Midgap D_{it}† $(10^{11}/cm^2\text{-eV})$	
						N_2 Anneal	H_2 Anneal	N_2 Anneal	H_2 Anneal
TR-1	900	O_2/-	300/0/0	O_2 FP	0.079	5.40	4.80	1.15	1.43
TR-2	"	O_2/-	300/0/10	O_2 SP	0.081	8.90	6.95	2.09	2.16
TR-3	"	O_2/N_2	300/10/2	N_2 SP	0.079	2.96	2.35	0.67	0.54
TR-4	"	O_2/Ar	300/10/2	Ar SP	0.081	2.97	3.55	0.76	0.46
TR-5	1000	O_2/-	84/0/0	O_2 FP	0.081	4.67	3.88	2.20	0.92
TR-6	"	O_2/-	84/0/10	O_2 SP	0.087	8.40	8.63	1.62	1.45
TR-7	"	O_2/N_2	84/10/2	N_2 SP	0.084	2.13	1.70	0.72	0.40
TR-8	"	O_2/Ar	84/10/2	Ar SP	0.084	1.84	1.81	0.38	0.25
TR-9	1100	O_2/-	28/0/0	O_2 FP	0.079	4.10	3.45	1.62	1.16
TR-10	"	O_2/-	28/0/10	O_2 SP	0.088	7.16	8.00	1.67	2.21
TR-11	"	O_2/N_2	28/10/2	N_2 SP	0.081	1.55	1.40	0.41	0.41
TR-12	"	O_2/Ar	28/10/2	Ar SP	0.082	1.75	1.80	0.34	0.38

* oxidation time/anneal time in N_2 or Ar/Pull time

** O_2 FP = fast pull (<3 sec) in O_2
O_2 SP = slow pull (10 min) in O_2
N_2 SP or Ar SP = slow pull (2 min) in N_2 or Ar

† measurements are carried out following post-metallization anneal in:
1) N_2 at 400°C for 10 min
2) 10% H_2 in N_2 at 400°C for 10 min

TABLE 4-2

Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) For P-Type (111) Silicon Wafers Oxidized in Dry Oxygen

Run No.	Oxidation Temp (°C)	Ox/ Anneal Ambient	Ox/ Anneal/Cool Time*(min)	Cool Condition**	Oxide Thickness (μm)	$N_f(10^{11}/cm^2)$†		Midgap D_{it}† $(10^{11}/cm^2\text{-eV})$	
						N_2 Anneal	H_2 Anneal	N_2 Anneal	H_2 Anneal
TR-21	900	O_2/-	300/0/0	O_2 FP	0.081	5.05	5.20	0.88	0.85
TR-22	"	O_2/-	300/0/10	O_2 SP	0.082	6.43	6.51	1.01	1.00
TR-23	"	O_2/N_2	300/10/2	N_2 SP	0.080	3.24	2.94	0.62	0.56
TR-24	"	O_2/Ar	300/10/2	Ar SP	0.081	3.31	3.32	0.52	0.59
TR-17	1000	O_2/-	84/0/0	O_2 FP	0.080	4.35	4.84	0.89	0.83
TR-18	"	O_2/-	84/0/10	O_2 SP	0.086	6.65	7.08	1.61	0.94
TR-19	"	O_2/N_2	84/10/2	N_2 SP	0.081	2.22	2.34	0.40	0.37
TR-20	"	O_2/Ar	84/10/2	Ar SP	0.080	2.47	2.60	0.37	0.45
TR-13	1100	O_2/-	28/0/0	O_2 FP	0.079	3.53	3.45	0.62	0.63
TR-14	"	O_2/-	28/0/10	O_2 SP	0.089	8.04	7.70	1.04	1.03
TR-15	"	O_2/N_2	28/10/2	N_2 SP	0.080	1.65	2.13	0.37	0.35
TR-16	"	O_2/Ar	28/10/2	Ar SP	0.080	1.44	1.50	0.36	0.35

* oxidation time/anneal time in N_2 or Ar/Pull time

** O_2 FP = fast pull (<3 sec) in O_2
O_2 SP = slow pull (10 min) in O_2
N_2 SP or Ar SP = slow pull (2 min) in N_2 or Ar

† measurements are carried out following post-metallization anneal in:
1) N_2 at 400°C for 10 min
2) 10% H_2 in N_2 at 400°C for 10 min

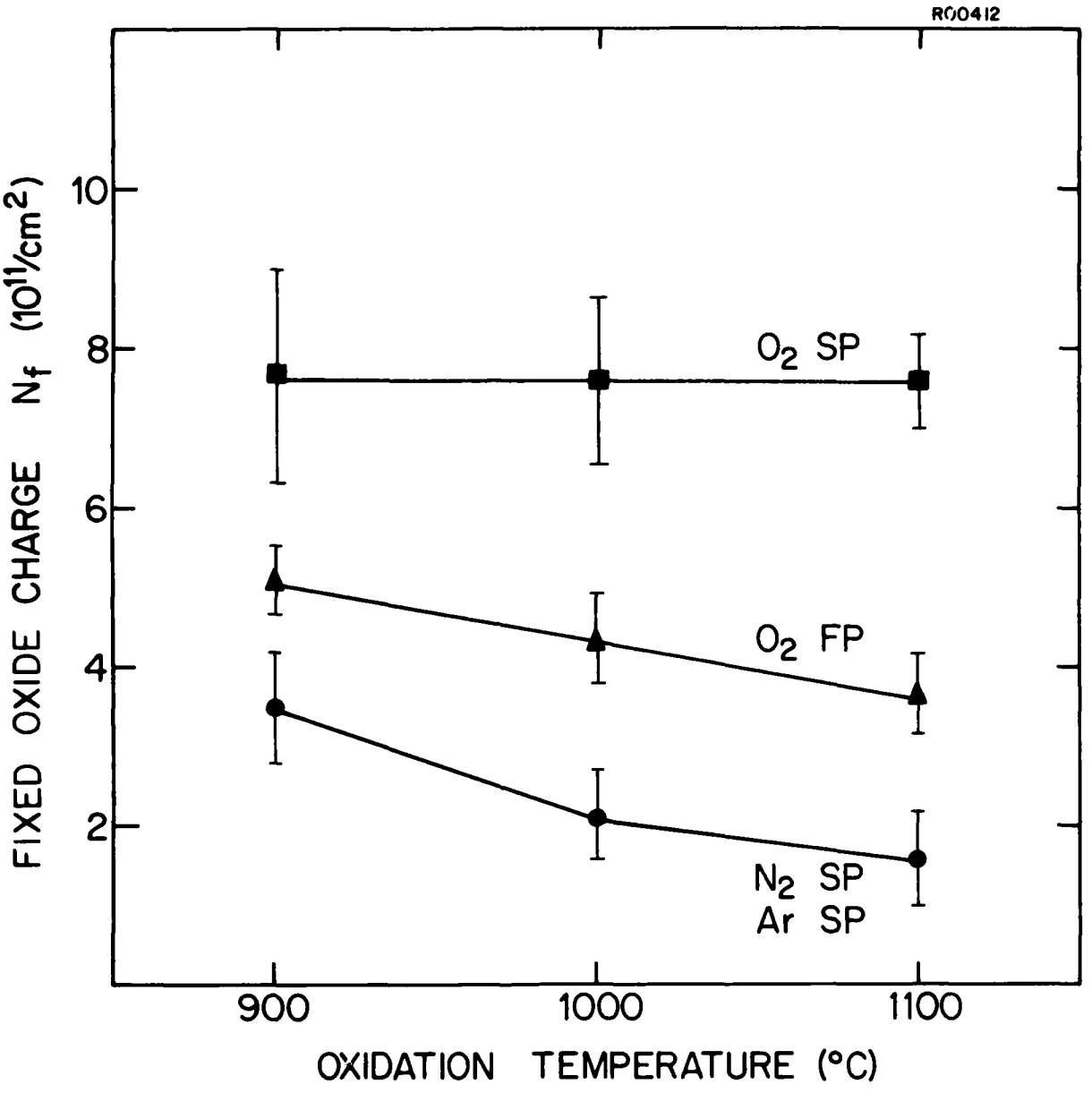

Fig. 4-1. Fixed oxide charge (N_f) versus oxidation temperature for n- and p-type (111) silicon wafers oxidized in dry O_2 and annealed/cooled in O_2, N_2, and Ar (N_2, Ar anneal time = 10 min). Oxide thickness x_o = 790-860 Å and post-metallization anneal (PMA) = 400°C/10% H_2 in N_2/10 min.

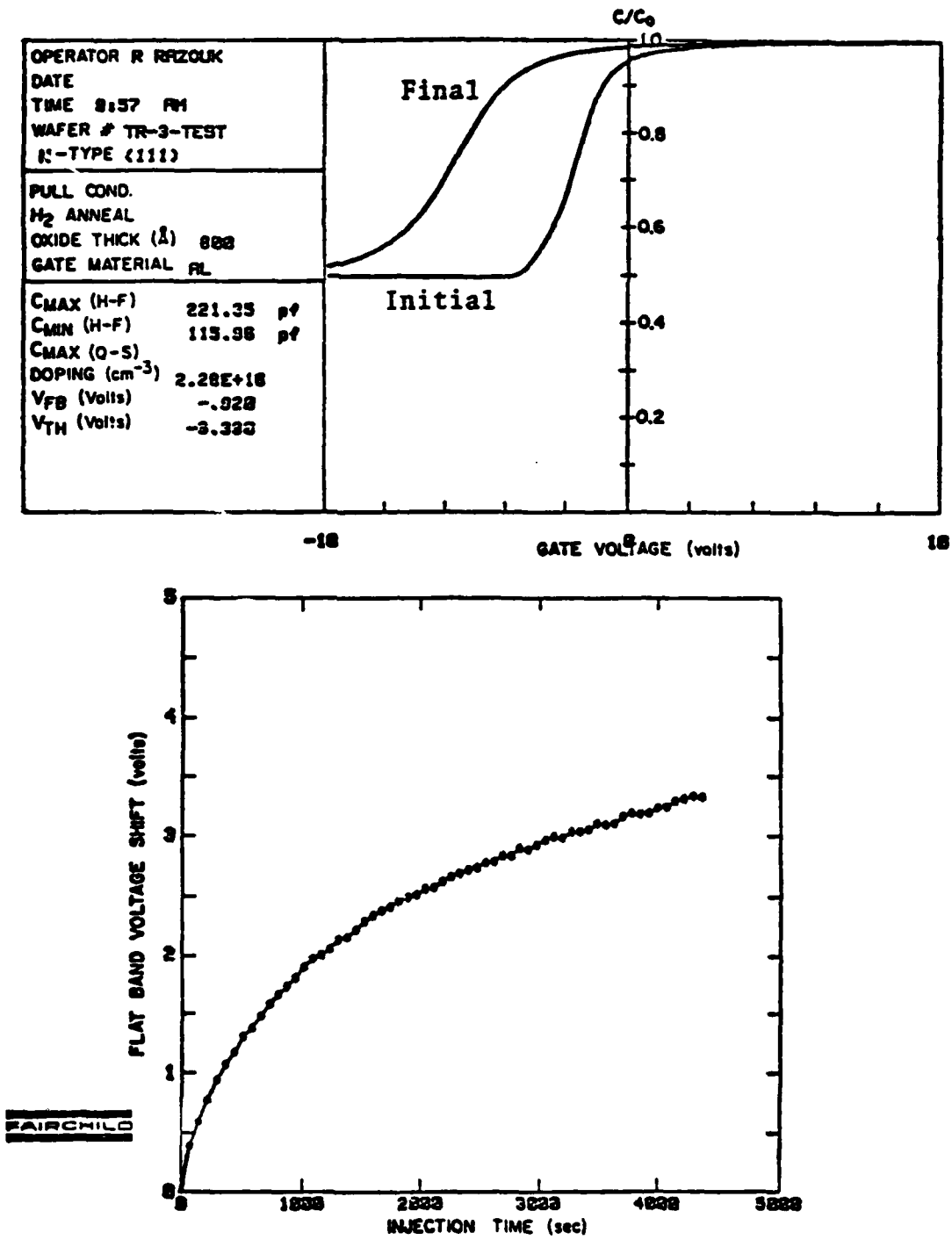

Fig. 4-2. Typical output from the automated avalanche carrier injection and trapping system.

The average current density used was 4.5×10^{-8} A/cm^2 for hole trapping from n-type substrates at a signal frequency of 45 KHz. The effect of anneal/cool ambients on hole trapping properties of oxides grown in dry O_2 at 1000°C is illustrated in Fig. 4-3. The least amount of trapping is found for samples cooled quickly (1-3 sec) in the oxidizing ambient (dry oxygen).

Comparisons between processes are done by recording the flat band voltage shift following 2000 sec of injection at the appropriate current density level. The results for avalanche hole trapping in n-type (111) silicon oxidized in dry O_2 are shown in Fig. 4-4. Post-oxidation in situ annealing is shown to increase trapping substantially at temperatures $\geq$1000°C. A small effect is noted for oxygen pulled samples with the best results obtained at 900°C.

Other information available from the measurement consists of capture cross sections and effective trap densities. For first order rate processes, the trapping-detrapping of thermal carriers can be expressed as:

$$\frac{dn_t}{dt} = \text{capture rate - detrapping by photons - detrapping by phonons}$$

$$\frac{dn_t}{dt} = n_c V_{th} \sigma_c (N-n_t) - F_p \sigma_p n_t - N_c n_t V_{th} \sigma_c \, e^{-E_t/kT} \qquad [1]$$

where

n_t = trapped charge density
N = total trap density
σ_c = capture cross section

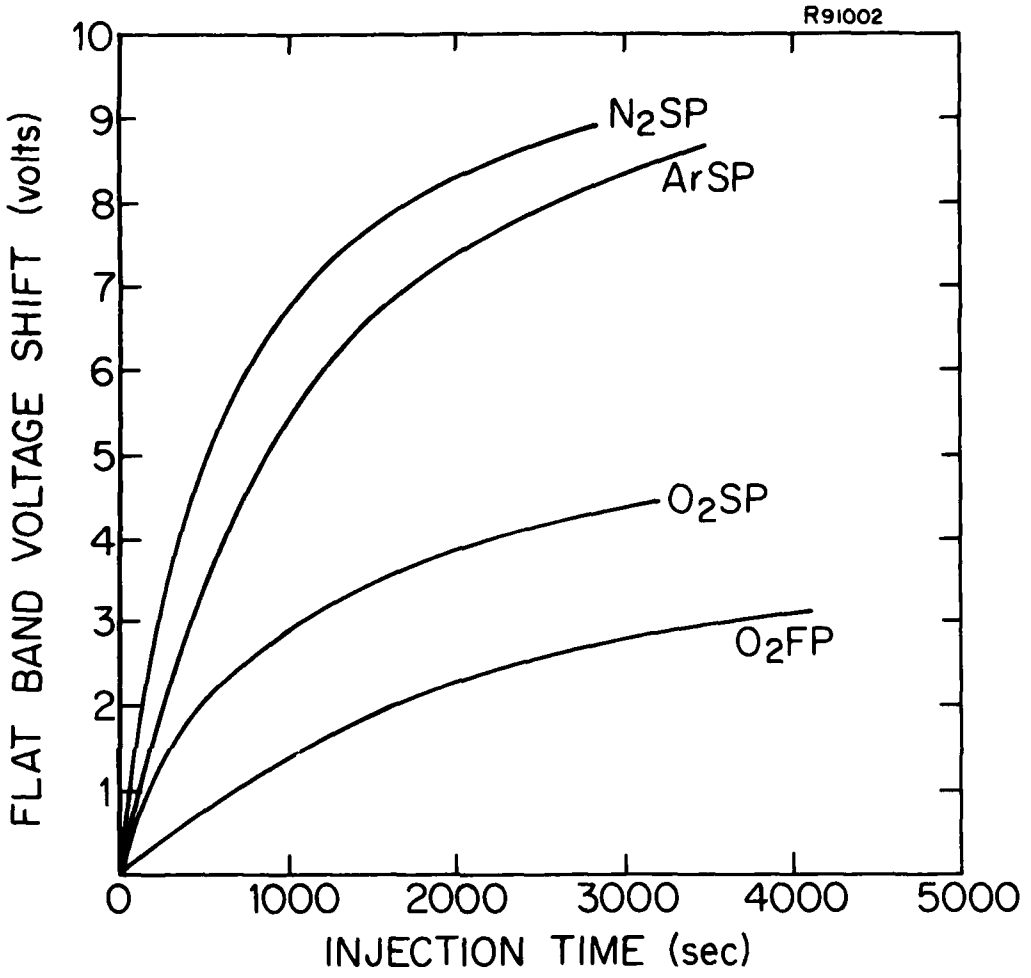

Fig. 4-3. Flat band voltage shift versus injection time for hole trapping from n-type (111) silicon oxidized in dry O_2 at 1000°C. Current density J = 4.5 x 10^{-8} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.

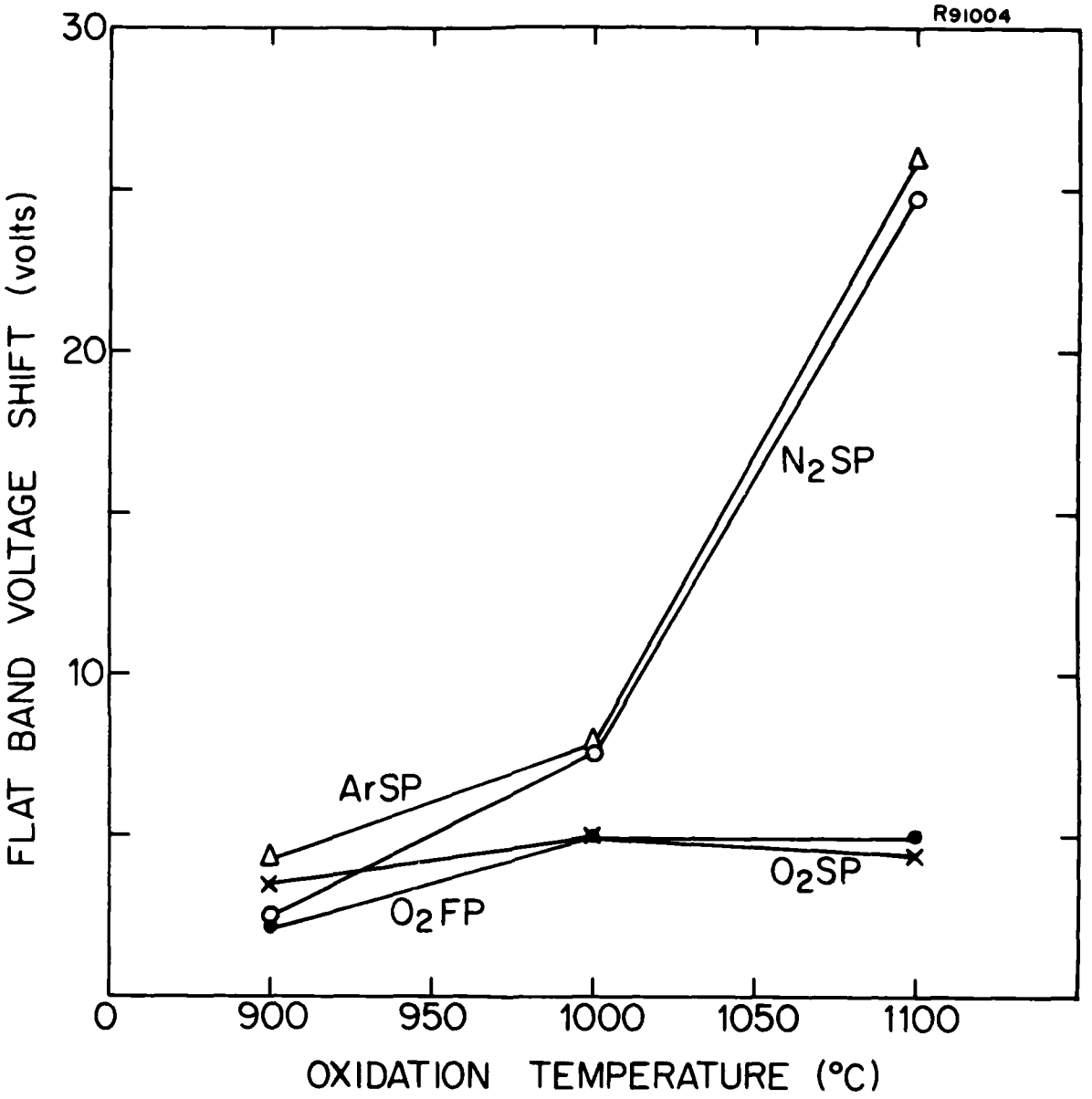

Fig. 4-4. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in dry O_2 and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 4.5×10^{-8} A/cm^2.

n_c = conduction band electron density
V_{th} = thermal velocity
F_p = photon flux
σ_p = photoionization cross section
N_c = effective density of states in the conduction band
E_t = trap energy depth from the conduction band edge

For cases where no detrapping is occurring, the trapping probability is proportional to the number of unfilled traps and the shift in flat band voltage is given by

$$\Delta V_{FB} = \frac{qN_{eff}}{C_{ox}} \left(1 - e^{-\sigma_c Jt/q}\right) \qquad [2]$$

where

ΔV_{FB} = flat band voltage shift
C_{ox} = oxide capacitance per unit area
J = current density
t = injection time
q = electronic charge
N_{eff} = effective charge density

by taking the derivative of [2] with respect to time

$$\frac{d}{dt}\left(\Delta V_{FB}\right) = \frac{d}{dt}\left(V_{FB}\right) = \frac{qN_{eff}}{C_{ox}}\left(\frac{\sigma_c J}{q}\right) e^{-\sigma_c Jt/q} \qquad [3]$$

and

$$\ln\left[\frac{d}{dt}\left(\Delta V_{FB}\right)\right] = \ln \frac{qN_{eff}}{C_{ox}}\left(\frac{\sigma_c J}{q}\right) - \left(\frac{\sigma_c J}{q}\right) t \qquad [4]$$

A plot of ln [d/dt (V_{FB})] versus injection time will yield a straight line in the case of a single trap. The slope of this line allows the computation of the capture cross section while the intercept gives information about the effective trap density. Although it is possible, if the measurement is carried out for long times (or by increasing the current density), to resolve more than one trapping cross section and trap density, the dominant trapping mechanism has been the primary objective of this investigation. A typical plot of ln [d/dt(V_{FB})] versus time is shown in Fig. 4-5 and indicates a trapping cross section of 3.5×10^{-15} cm^2 and an effective trap density of $2 \times 10^{12}/cm^2$.

The variations in the result from capacitor to capacitor on the same wafer and wafer to wafer on the same run were minor. Some variations were noted from run to run under identical processing conditions; however, these variations were substantially lower than the 4:1 ratio observed by Aitken and Young (35) between some of their batches. These differences have also been reported by G. W. Hughes (39) who found occasional large variation in radiation hardness from wafer to wafer as well as from run to run under identical processing conditions and by H. L. Hughes (40) who found correlation between silicon surface defects as revealed by Sirtl etch and radiation hardness in MOS structures.

Interface state generation was observed for most samples tested and resulted in a stretch out of the C-V curves. Quasi-static C-V measurements indicated interface state density increases up to the $10^{12}/cm^2$-eV at midgap. The exact nature of the increase in interface states is not known at this time since the trapped charges at the Si-SiO_2 interface could by virtue of their presence or nonuniform distribution result in an "apparent" increase in interface states. The deconvolution of the various contributions could probably be best carried

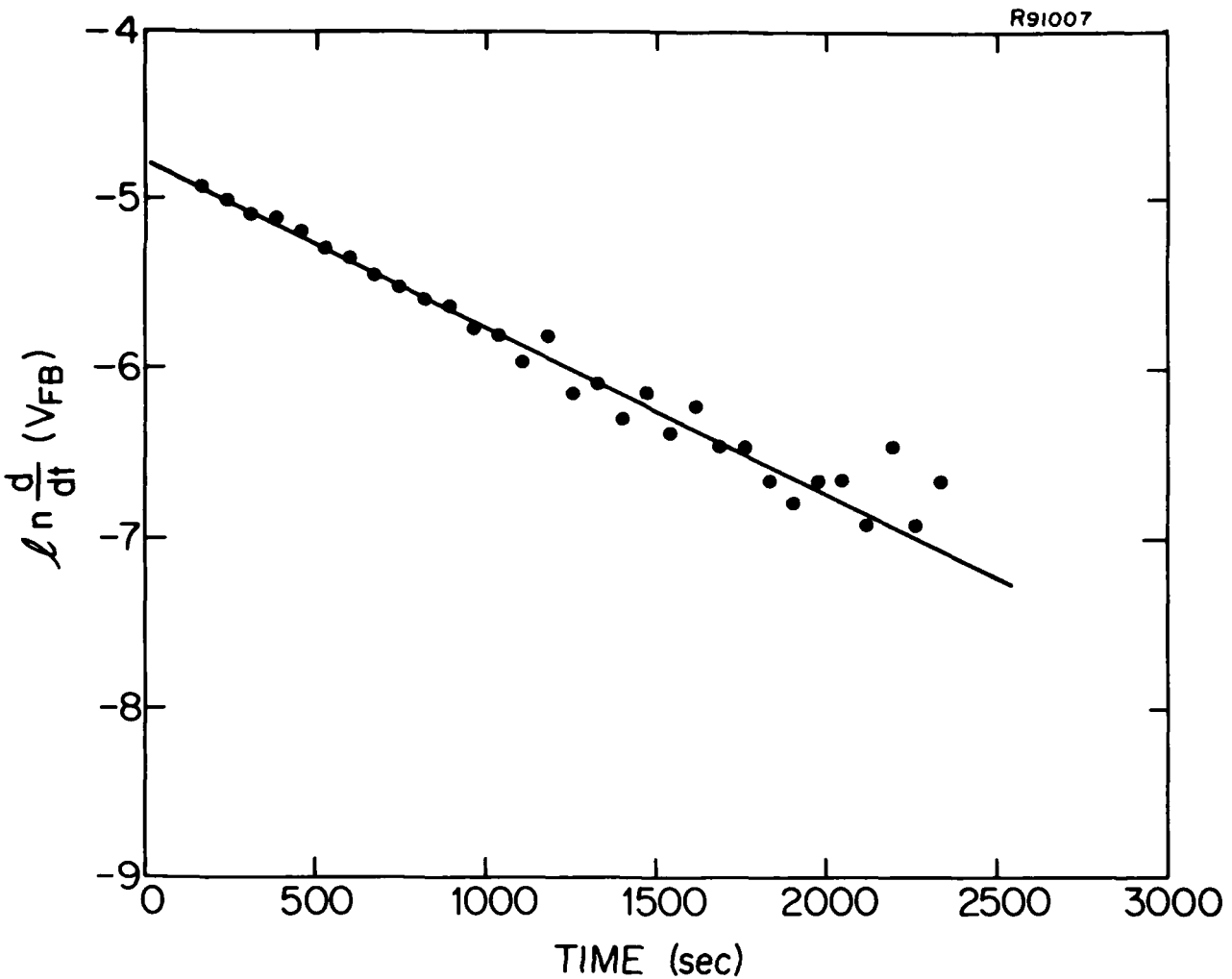

Fig. 4-5. ℓn d/dt (V_{FB}) versus time for a sample oxidized in dry O_2 at 1000°C. The sample received an in situ anneal in nitrogen for 10 min and was cooled in N_2. The post metallization anneal treatment was: 400°C, 10% H_2 in N_2, 10 min. Current density J = 4.5 x 10^{-8} A/cm^2.

out through annealing treatments known to affect only one of the two charges in question.

One of the main objectives of this program is the characterization of the interrelationship between avalanche injected charge trapping and radiation induced charge trapping. This objective was carried out by sending samples processed simultaneously with the avalanche injection samples to H. L. Hughes at the Naval Research Laboratories. In the case of n-type (111) samples (used for hole avalanche trapping) the wafers were exposed to 1 x 10^6 rads with a positive bias of 10 volts. Figure 4-6 shows the measured changes in inversion voltage versus dry O_2 oxidation temperature for four cooling conditions. These results are in excellent agreement with the hole trapping by avalanche injection data presented in Fig. 4-4. The results suggest that the traps are strongly process dependent but unrelated to the method by which the trapped carriers are made available be it ionizing radiation or injection over the barrier due to avalanche.

4.1.2 Electron Trapping in Dry O_2

Electron injection was carried out from p-type (111) substrates by avalanche injection. The same process conditions investigated for hole trapping were used and the oxide thickness, capacitor area, and signal frequency were the same (800 Å, 4.5 x 10^{-3} cm^2, and 45 KHz). The average current density was 1.5 x 10^{-5} A/cm^2. The process dependence of electron trapping is summarized in Fig. 4-7 and indicates the following:

(a) The electron trapping efficiency as evidenced by the average current and change in flat band voltage is much lower than the hole trapping efficiency as reported in the literature.

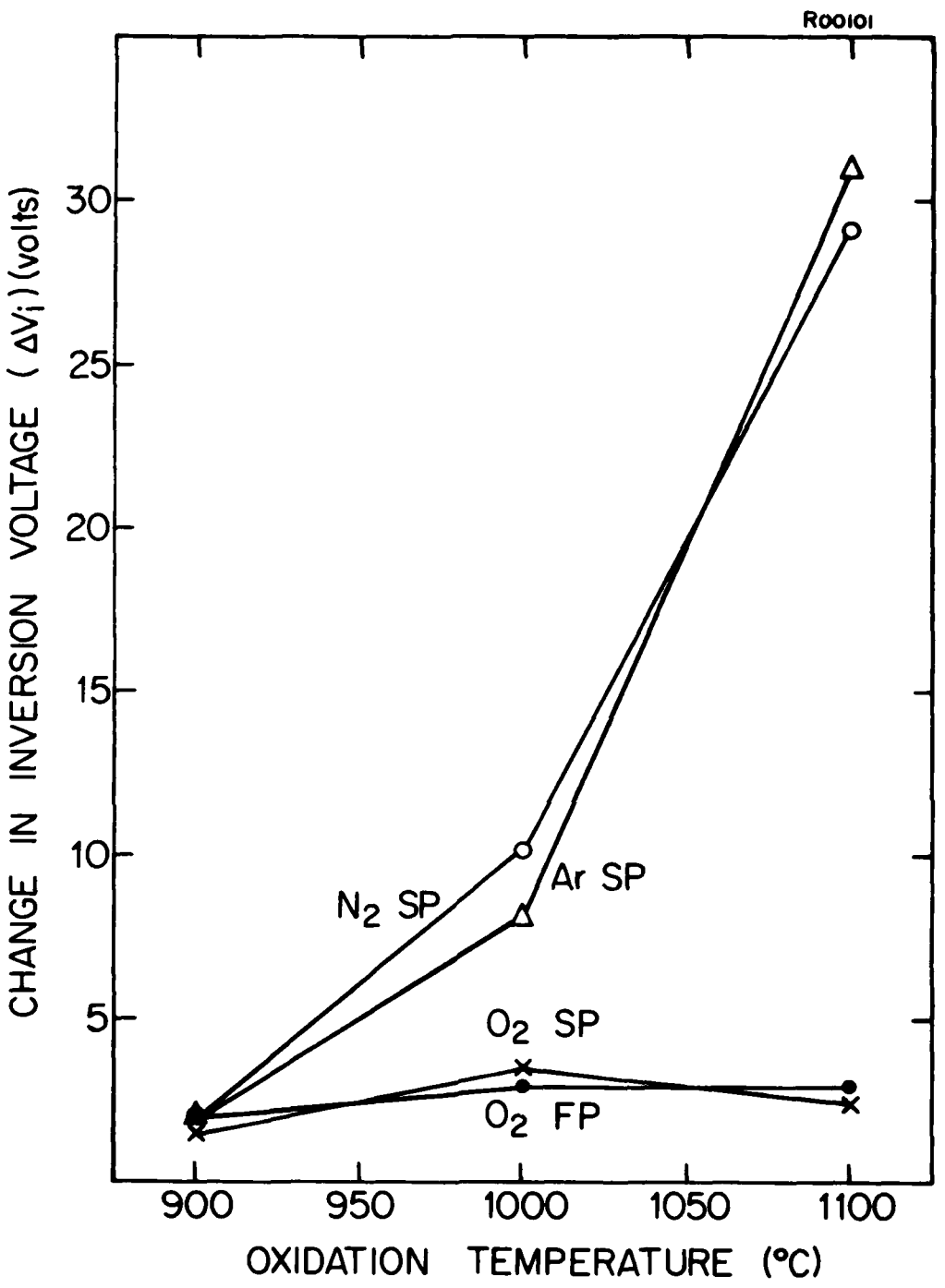

Fig. 4-6. Change in inversion voltage following irradiation versus oxidation temperature for hole trapping from n-type (111) substrates. Samples were oxidized in dry O_2 and received a post-metallization anneal at 400°C, in a 10% H_2 in N_2 ambient for 10 minutes. Irradiation parameters: 10^6 Rads, +10 V.

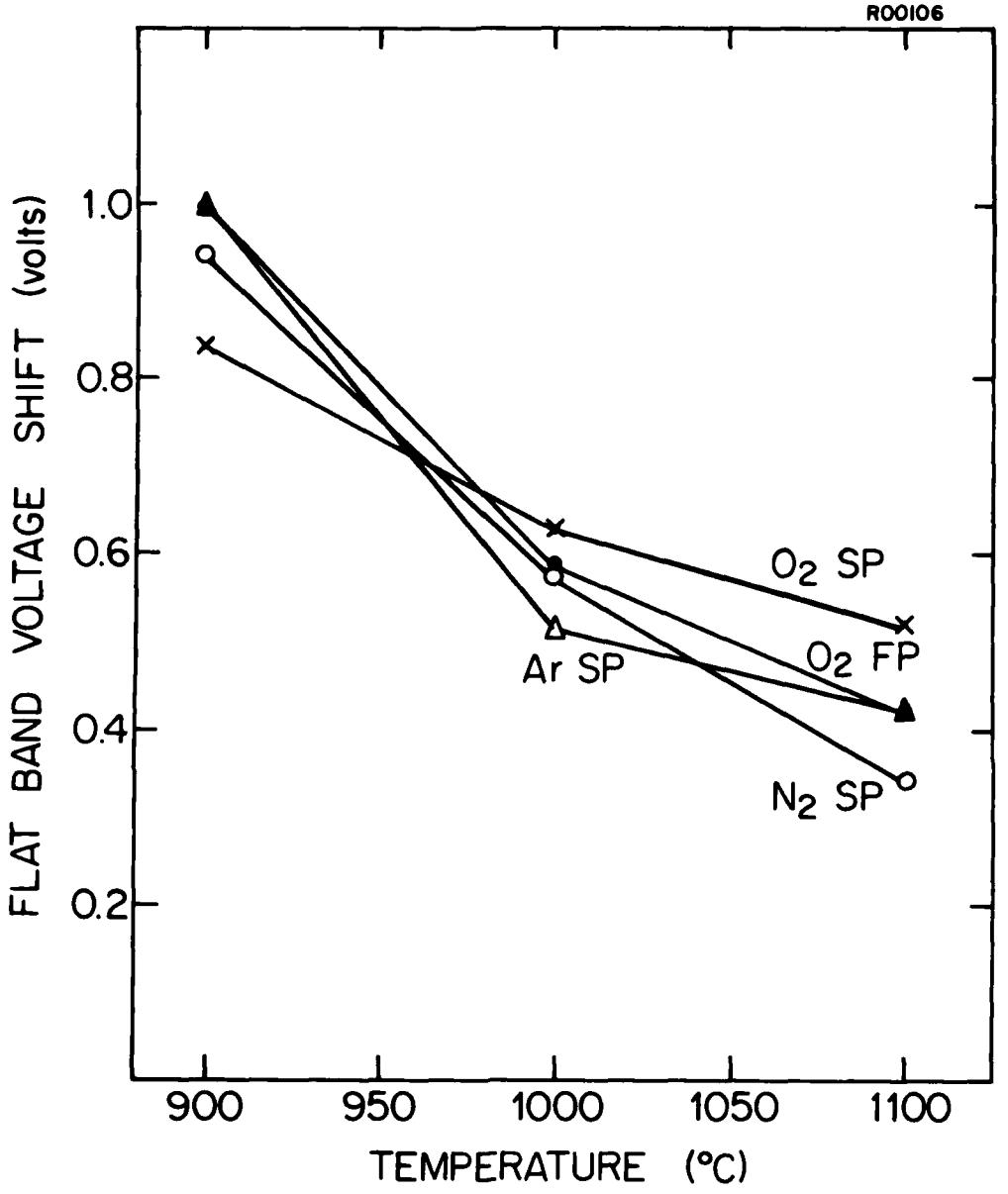

Fig. 4-7. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (111) substrates. Samples were oxidized in dry O_2 and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 1.5 x 10^{-5} A/cm^2.

(b) The least amount of trapping occurs at higher oxidation temperatures (1100°C).

(c) Variations in post-oxidation anneal ambients and cooling rates have a minor effect on the amount of flat band voltage shift observed.

The density of interface traps or states generated during avalanche injection is illustrated in Fig. 4-8 for sample TR22-H. The starting level of fixed oxide charge was approximately $6.5 \times 10^{11}/cm^2$. Following avalanche injection flat band voltage changes reflect the trapping of electrons, generation of interface states, and the initial level of fixed oxide charge. Due to electron trapping and/or interface state generation the "effective" oxide charge is seen to drop while the level of interface states at midgap increases from less than 1×10^{11} to about $1 \times 10^{12}/cm^2$-eV. However, no separation of the various charge contributions is possible at this time.

Typical values of capture cross section and effective trap density were around 3×10^{-18} cm^2 and $6 \times 10^{11}/cm^2$ respectively for oxides prepared at 900°C.

4.2 Trapping in Pyrogenic Steam Oxides

N- and p-type (111) silicon wafers, run numbers TR-25 through TR-42, were oxidized in pyrogenic steam at 900°, 1000°, and 1100°C. Fixed oxide charge and interface state density charge levels prior to avalanche charge injection are tabulated in Tables 4-3 and 4-4. Argon and N_2 post-oxidation anneals are shown to reduce the level of fixed oxide charge and interface trapped charge at all temperatures in a manner similar to that observed in dry O_2 oxides.

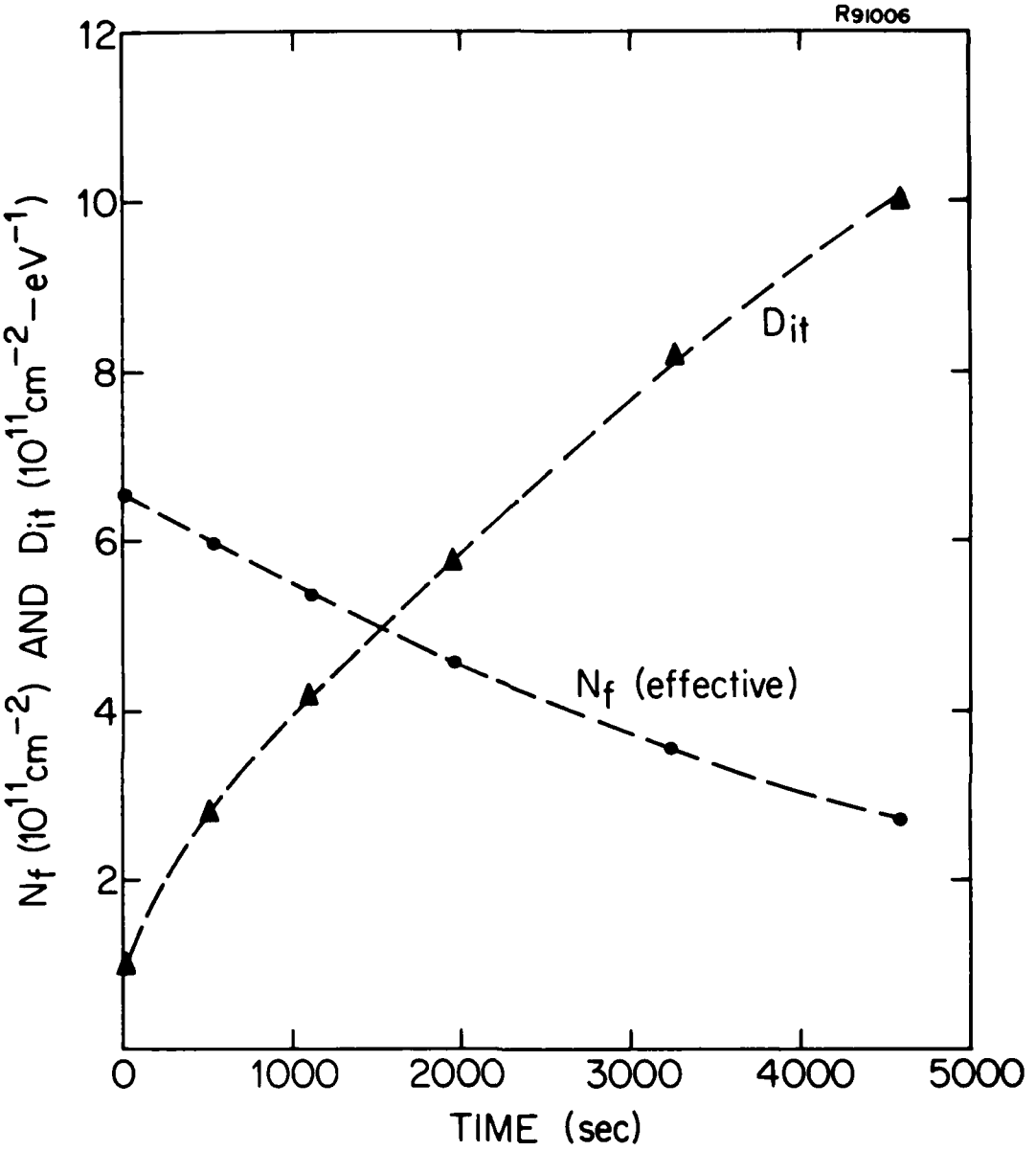

Fig. 4-8. Effective fixed oxide charge density (N_f) and interface trapped charge density (D_{it}) versus electron avalanche injection time. Samples were oxidized in dry O_2 at 900°C and cooled slowly in oxygen (O_2 SP).

TABLE 4-3

Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) For N-Type (111) Silicon Wafers Oxidized in Steam

Run No.	Oxidation Temp. (°C)	Ox/ Anneal Ambient	Ox/ Anneal/Cool Time*(min)	Cool Condition**	Oxide Thickness (μm)	$N_f(10^{11}/cm^2)$†		Midgap D_{it}† $(10^{11}/cm^2\text{-eV})$	
						N_2 Anneal	H_2 Anneal	N_2 Anneal	H_2 Anneal
TR-25	900	H_2O/-	20/0/0	H_2O FP	0.082	4.10	4.03	0.90	1.17
TR-26	"	H_2O/N_2	20/10/2	N_2 SP	0.083	2.43	2.38	0.43	0.45
TR-27	"	H_2O/Ar	20/10/2	Ar SP	0.083	2.80	2.40	0.34	0.47
TR-28	1000	H_2O/-	5/0/0	H_2O FP	0.080	3.50	3.63	0.56	0.62
TR-29	"	H_2O/N_2	5/10/2	N_2 SP	0.082	2.17	1.71	0.32	0.31
TR-30	"	H_2O/Ar	5/10/2	Ar SP	0.081	2.67	2.27	0.23	0.40
TR-31	1100	H_2O/-	1.75/0/0	H_2O FP	0.087	3.81	4.12	0.78	0.84
TR-32	"	H_2O/N_2	1.75/10/2	N_2 SP	0.087	1.80	1.62	0.26	0.24
TR-33	"	H_2O/Ar	1.75/10/2	Ar SP	0.087	1.78	1.76	0.40	0.30

* oxidation time/anneal time in N_2 or Ar/pull time

** H_2O FP = fast pull (<3 sec) in H_2O
N_2 SP or Ar SP = slow pull (2 min) in N_2 or Ar

† measurements are carried out following post-metallization anneal in:
1) N_2 at 400°C for 10 min
2) 10% H_2 in N_2 at 400°C for 10 min

TABLE 4-4

Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) For P-Type (111) Silicon Wafers Oxidized in Steam

Run No.	Oxidation Temp. (°C)	Ox/ Anneal Ambient	Ox/ Anneal/Cool Time*(min)	Cool Condition**	Oxide Thickness (μm)	$N_f(10^{11}/cm^2)$†		Midgap D_{it}† $(10^{11}/cm^2\text{-eV})$	
						N_2 Anneal	H_2 Anneal	N_2 Anneal	H_2 Anneal
TR-40	900	H_2O/-	20/0/0	H_2O FP	0.080	4.68	4.48	0.92	0.68
TR-41	"	H_2O/N_2	20/10/2	N_2 SP	0.080	3.00	3.43	0.51	0.48
TR-42	"	H_2O/Ar	20/10/2	Ar SP	0.082	3.50	4.00	0.70	1.30
TR-37	1000	H_2O/-	5/0/0	H_2O FP	0.077	4.78	4.39	0.87	0.64
TR-38	"	H_2O/N_2	5/10/2	N_2 SP	0.080	1.90	2.05	0.46	0.37
TR-39	"	H_2O/Ar	5/10/2	Ar SP	0.077	2.24	2.20	0.44	0.45
TR-34	1100	H_2O/-	1.75/0/0	H_2O FP	0.078	4.65	4.39	0.75	0.55
TR-35	"	H_2O/N_2	1.75/10/2	N_2 SP	0.088	2.26	2.17	0.65	0.55
TR-36	"	H_2O/Ar	1.75/10/2	Ar SP	0.081	2.26	1.83	0.68	0.45

* oxidation time/anneal time in N_2 or Ar/pull time

** H_2O FP = fast pull (<3 sec) in H_2O
N_2 SP or Ar SP = slow pull (2 min) in N_2 or Ar

† measurements are carried out following post-metallization anneal in:
1) N_2 at 400°C for 10 min
2) 10% H_2 in N_2 at 400°C for 10 min

4.2.1 Hole Trapping in Steam Oxides

Typical flat band voltage shift versus injection time plots for steam grown oxides are shown in Fig. 4-9. Oxides cooled in the steam ambient are characterized by increased trapping, and post oxidation anneals play a dominant role by reducing charge trapping and interface state density generation to dry O_2 levels. It is notable that Ar anneals are very similar to N_2 anneals in all the hole trapping data gathered in this investigation.

A summary of the hole trapping data is presented in Fig. 4-10. Steam oxidations result in increased trapping for all three temperatures investigated. Post oxidation anneals in either Ar or N_2 result in substantial reductions in trapping at 900° and 1000°C to dry O_2 oxide levels. At 1100°C, however, the data are almost identical to the dry O_2 data reconfirming the deleterious effect of post oxidation anneals at 1100°C. This result is the more interesting because 1100°C post-oxidation N_2 and Ar anneals are typically characterized by a minimum level of both oxide fixed charge and interface state density. Furthermore Ar is more inert than N_2 and a reaction with the substrate seems unlikely. This behavior is in sharp contrast with electron trapping observations discussed in the following section. No differences were observed between post-metallization sintering in N_2 and anneal in forming gas at 400°C for 10 min.

4.2.2 Electron Trapping in Steam Oxides

Characteristic of electron trapping in steam oxides is the anomalous decrease in flat band voltage shift observed for wafers cooled in steam. Figure 4-11 illustrates this effect at 1000°C. This decrease in flat band voltage shift has been observed previously (19) and it has been proposed that interface state

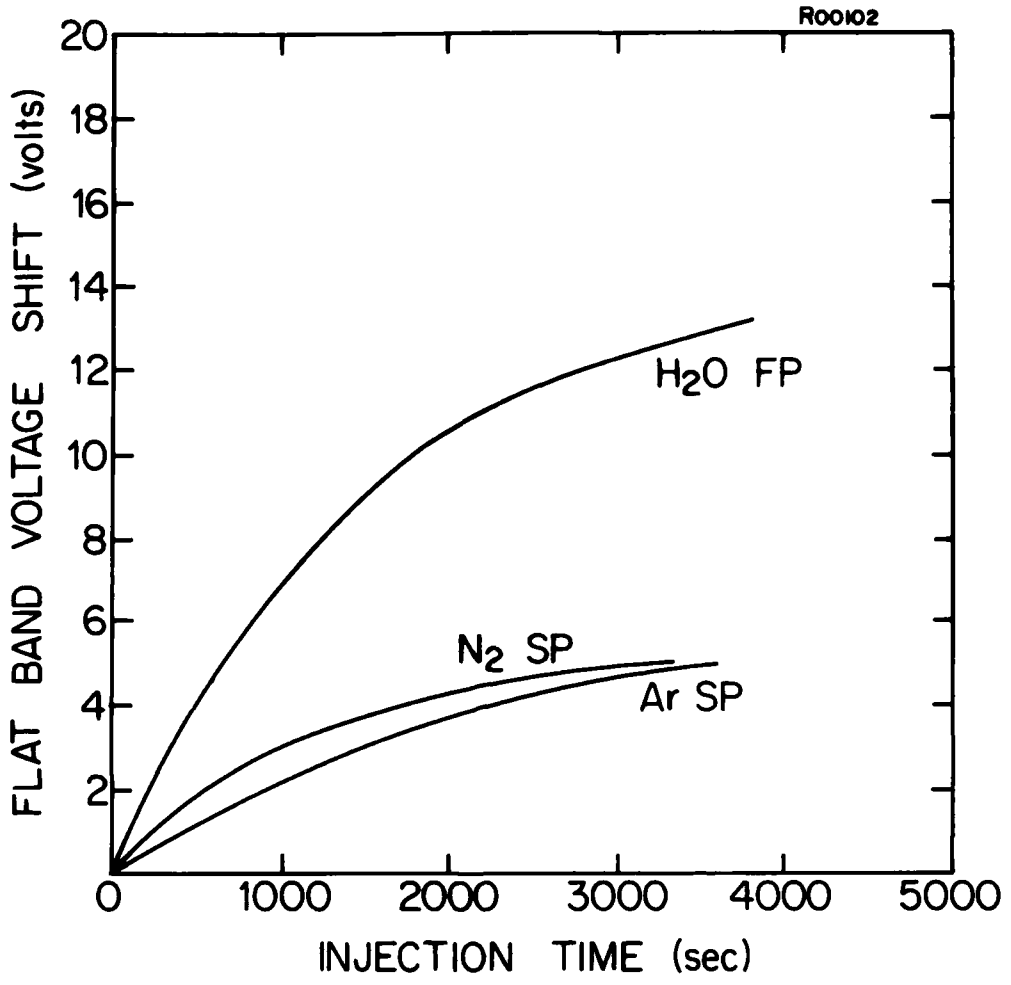

Fig. 4-9. Flat band voltage shift versus injection time for hole trapping from n-type (111) silicon oxidized in pyrogenic steam at 1000°C. Current density J = 4.5×10^{-8} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.

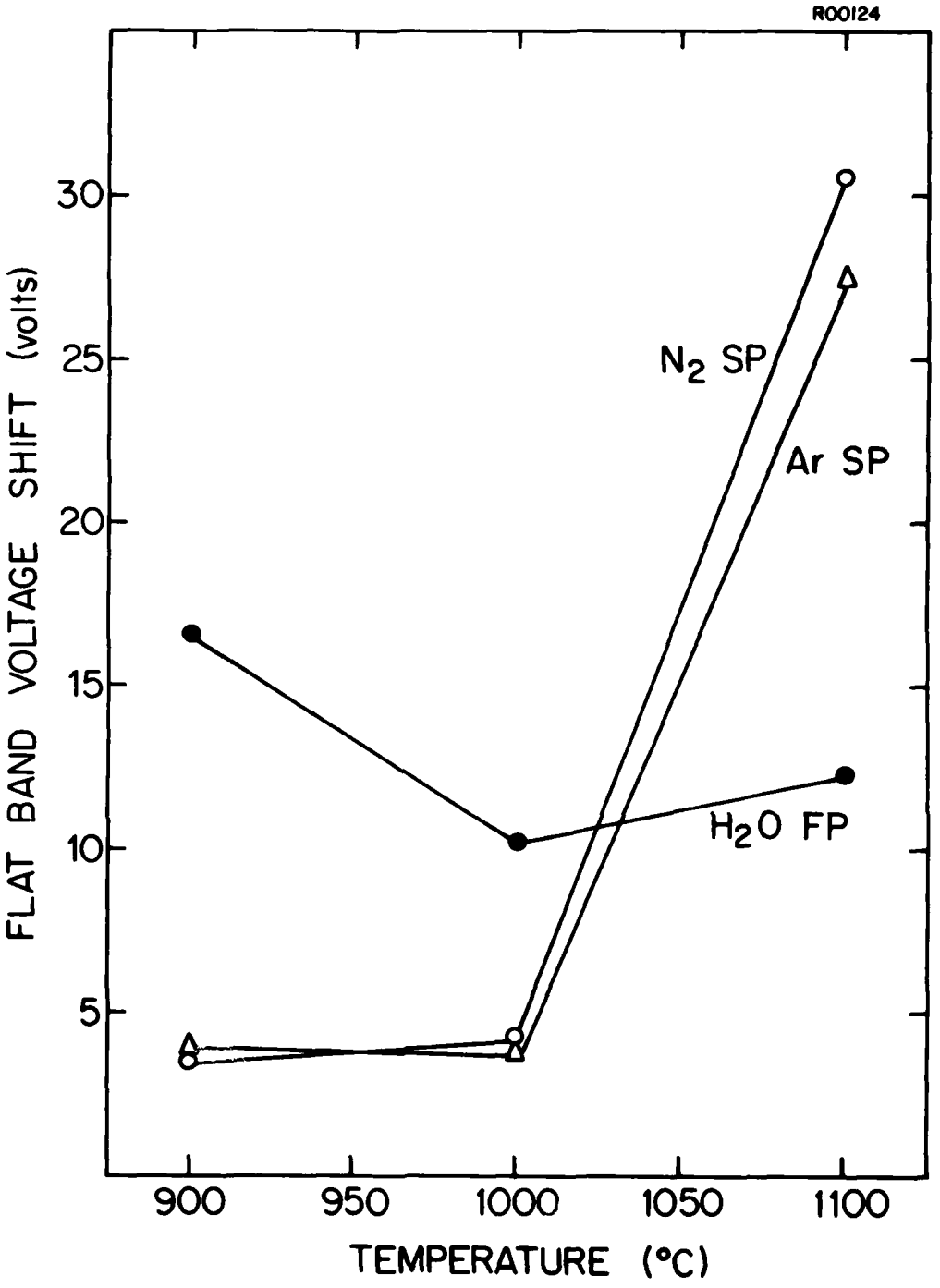

Fig. 4-10. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in steam and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density J = 4.5×10^{-8} A/cm^2.

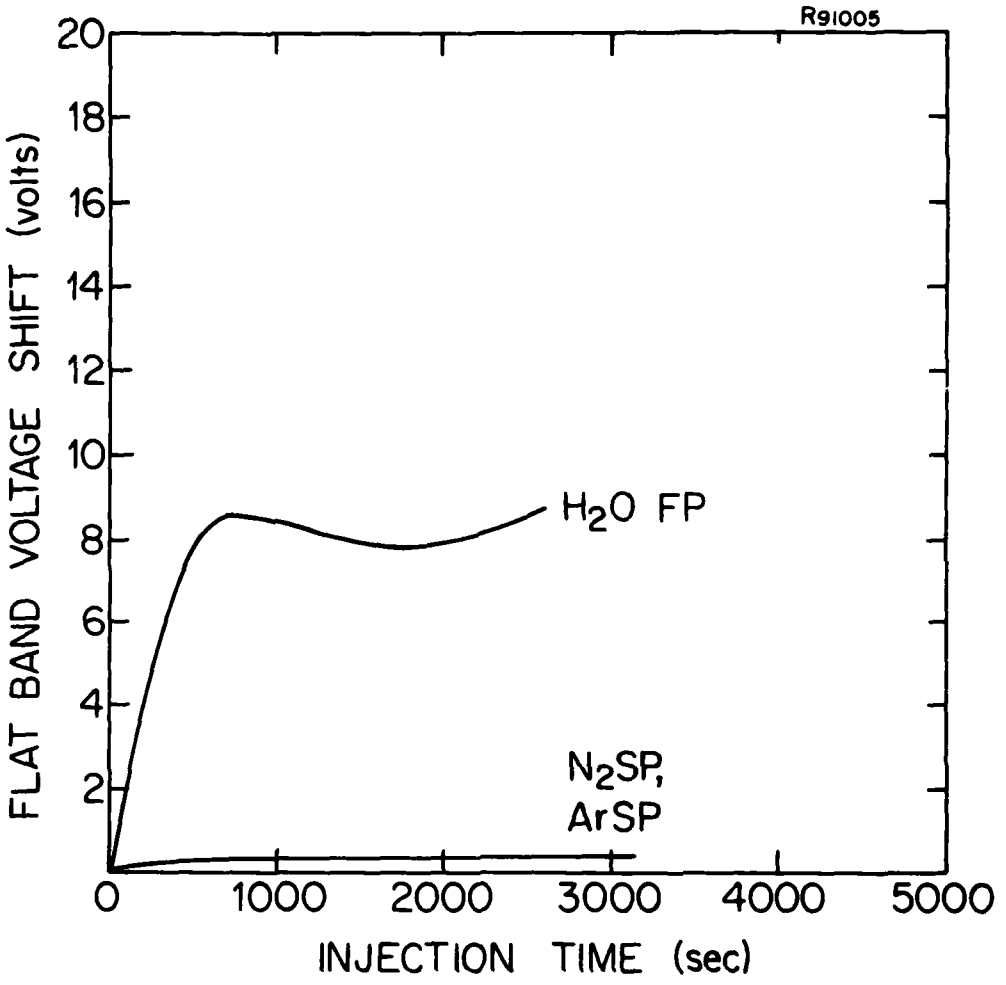

Fig. 4-11. Flat band voltage shift versus injection time for electron trapping from p-type (111) silicon oxidized in pyrogenic steam at 1000°C. Current density J = 1.5 x 10^{-5} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.

generation may be the reason. Quasistatic C-V as well as high frequency measurements carried out on these samples indicate high levels of interface states are generated prior to the decrease in flat band voltage. These states could of course be a manifestation of nonuniform charge densities at the interface. In any event, the flat band voltage decrease seems to occur when a significant number of donor-like states are generated, particularly below midgap.

Nitrogen and argon post-oxidation anneal result in a substantial decrease in trapping particularly at 1000°C and above. A summary of electron trapping data is presented in Fig. 4-12. The high levels of trapping following post-oxidation anneal in N_2 or Ar at 900°C are worth noting. Longer anneal times at the lower temperatures may be needed to reduce trapping. Also of importance is the decrease in trapping with increasing temperature and with inert gas anneals at all temperatures. This behavior is typical of fixed oxide charge both in dry O_2 and in steam oxides. Some correlation seem to be present between electron trapping and the levels of positive fixed oxide charge particularly in dry oxides or oxides annealed in N_2 or Ar. Electron trapping could be occurring both on water related sites and possibly on positive fixed charge sites.

As with previous results no differences were observed between post metallization sintering in N_2 and anneal in forming gas at 400°C for 10 minutes.

4.3 Trapping in O_2/HCl Oxides

N- and p-type (111) silicon wafers, runs TR-43 through TR-46 were oxidized in a 5% HCl/O_2 ambient at 1000°C. All wafers received a 15 minute post oxidation in situ anneal in argon or nitrogen. Table 4-5 summarizes the oxide charges N_f and D_{it} at midgap for the four runs.

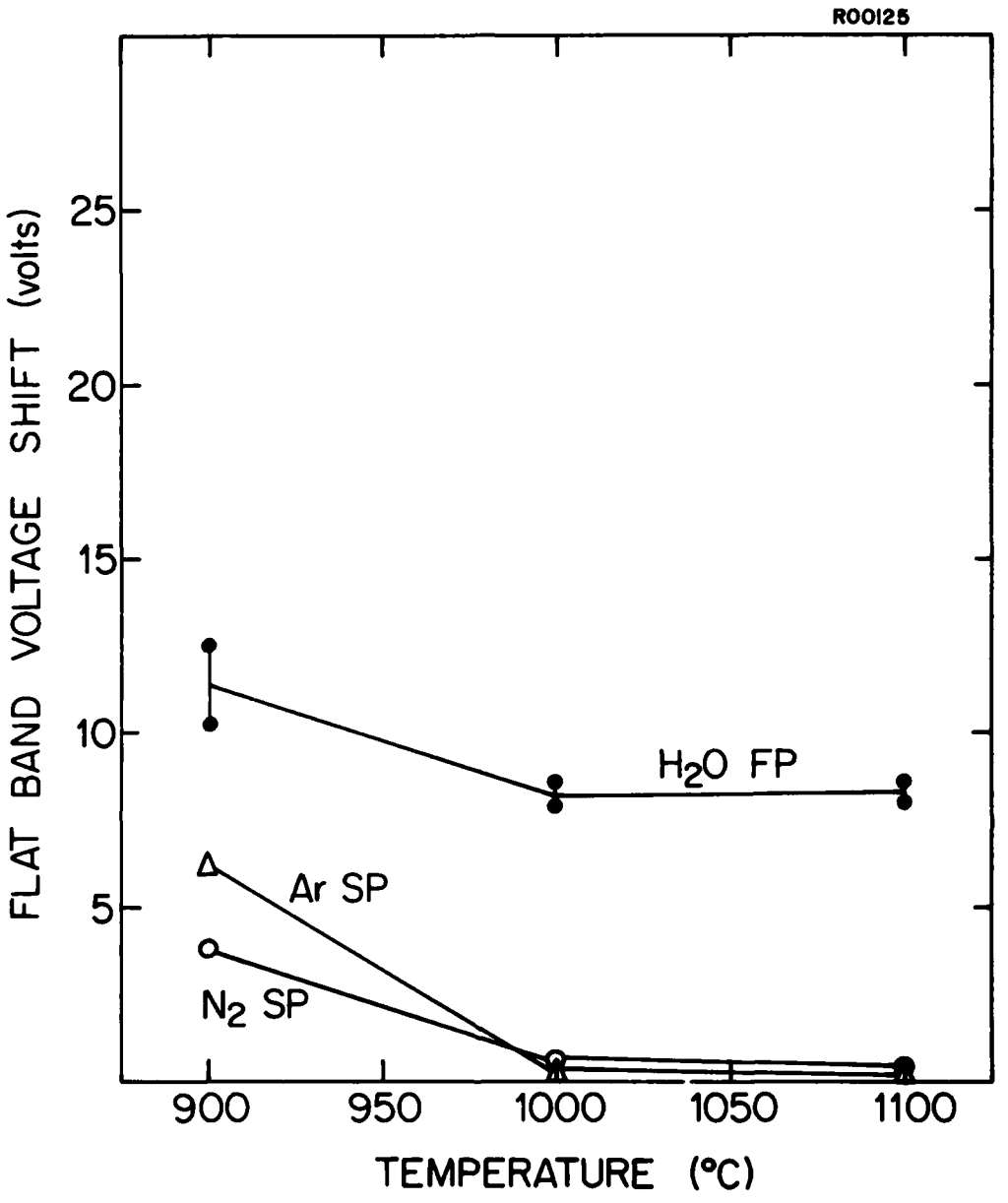

Fig. 4-12. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (111) substrates. Samples were oxidized in steam and received a post metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 minutes. Flat band voltage shifts are for 2000 sec injection time. Current density = J 1.5×10^{-5} A/cm^2.

TABLE 4-5

Values of Fixed Oxide Charge (N_f) and Interface State Density (D_{it}) for P- and N-Type (111) Silicon Wafers Oxidized in 5% HCl/O_2 at 1000°C

Run No.	Wafer Type Orient.	Ox/ Anneal Ambient	Ox/ Anneal/Cool Time*(min)	Cool Condition**	Oxide Thickness (μm)	$N_f(10^{11}/cm^2)$ †		Midgap D_{it} † $(10^{11}/cm^2\text{-eV})$	
						N_2 Anneal	H_2 Anneal	N_2 Anneal	H_2 Anneal
TR-43	N-(111)	5% HCl/O_2	49/10/2	Ar SP	0.079	2.41	2.30	0.42	0.40
TR-44	N-(111)	"	"	N_2 SP	0.081	2.42	2.20	0.44	0.42
TR-45	P-(111)	"	"	Ar SP	0.079	2.66	2.75	0.43	0.43
TR-46	P-(111)	"	"	N_2 SP	0.081	2.78	2.78	0.43	0.41

* oxidation time/anneal time in N_2 or Ar/pull time

** H_2O FP = fast pull (<3 sec) in H_2O
N_2 SP or Ar SP = slow pull (2 min) in N_2 or Ar

† measurements are carried out following post-metallization anneal in:
1) N_2 at 400°C for 10 min
2) 10% H_2 in N_2 at 400°C for 10 min

4.3.1 Hole Trapping in 5% HCl/O_2 Oxides

Flat band voltage shifts exceeding 16 volts (average current density 4.5×10^{-8} A/cm^2, 45 KHz, 2000 sec) were recorded; the highest for hole trapping at 1000°C. Differences between Ar and N_2 post-oxidation anneals were minor. The increased trapping in the samples is clearly related to the chlorine presence in the oxide, predominantly at the $Si-SiO_2$ interface since trapping due to water related sites, a by-product of the O_2/HCl reaction, was shown to be minimized following a 10 minute N_2 or Ar anneal at 1000°C. Even though the presence of chlorine at the $Si-SiO_2$ interface does not seem to have a considerably effect on fixed oxide charge and interface states, it could act as traps for holes injected from the substrate.

Interface state density increases were also observed during avalanche hole injection and typically exceeded 10^{12}/cm^2-eV at midgap.

4.3.2 Electron Trapping in 5% HCl/O_2 Oxides

Electron trapping characteristics differed substantially once more from hole trapping characteristics. Flat band voltage shifts of approximately 1 volt were observed. Results were similar to dry O_2 oxides or H_2O oxides annealed in N_2 or Ar. The positive oxide charges were slightly higher than in dry O_2 and H_2O oxides and this correlates quite well with slightly higher trapped charge following the 2000 sec injection time. Interface state density generation was also observed on all the samples tested.

5.0 SUMMARY AND CONCLUSIONS

Characterization of the process dependence of avalanche injected electrons and holes in thermally grown silicon dioxide has been completed. Process parameters investigated included oxidation ambient (O_2, H_2O, and O_2/HCl), post-oxidation in situ anneal ambient (N_2, Ar), cooling ambient (O_2, N_2, and Ar), cooling rates (<3 sec, 2 min, and 10 min), and post-metallization anneals (N_2, N_2/H_2). The major conclusions from this part of the investigation are summarized below:

A. Basic differences exist between the process dependence of electron and hole trapping in thermally grown SiO_2.

B. Excellent agreement exists between hole trapping in dry O_2 due to avalanche injection and ionizing radiation.

C. Some general characteristics of hole trapping are:

   1. minimum in dry O_2 oxides,

   2. increases for N_2 anneals at $\geq$1000°C,

   3. high for steam oxides but is reduced by N_2 or Ar anneals at $\leq$1000°C,

   4. highest in 5% HCl/O_2 oxides.

D. Some general characteristics of electron trapping are:

   1. minimum for dry O_2 at 1100°C,

   2. highest for steam oxides but is reduced by N_2 or Ar anneals at all temperatures--best at 1100°C,

3. seems to be related to fixed oxide charges in some cases, namely where post oxidation anneals are involved.

E. No difference was noted between N_2 post-metallization sintering and N_2/H_2 forming gas anneal for both electron and hole trapping.

During the next phase of the program, the investigation effort will be concentrated on (100) silicon. In addition to dry O_2 and steam oxidations, high pressure oxidation will be investigated. Also, effects of radiation producing processes such as electron beam evaporation and sputter metallization will be surveyed.

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REFERENCES

(1) W. A. Pliskin and R. A. Gdula, in "Handbook of Semiconductors," S. Keller, Ed., Vol. 3, Elsevier-North Holland Publishing Co., New York, to be published.

(2) R. Champagne and M. Toole, Solid-State Tech. 20, 61 (1977).

(3) B. E. Deal and A. S. Grove, J. Appl. Phys. 36, 3770 (1965).

(4) B. E. Deal, J. Electrochem. Soc. 121, 198C (1974).

(5) B. E. Deal in "Semiconductor Silicon 1977," H. R. Huff and E. Sirtl, Eds., pp. 276-296, The Electrochemical Society, Inc., Princeton, New Jersey (1977).

(6) P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, J. Appl. Phys. 50, 5847 (1979).

(7) B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, J. Electrochem. Soc. 114, 266 (1967).

(8) D. R. Lamb and F. R. Badcock, Int. J. Electronics 24, 11 (1968).

(9) F. Montillo and P. Balk, J. Electrochem. Soc. 118, 1463 (1971).

(10) W. M. Werner, J. Electrochem. Soc. 123, 540 (1976).

(11) R. R. Razouk and B. E. Deal, J. Electrochem. Soc. 126, 1573 (1979).

(12) R. Williams, Phys. Rev. 140, A569 (1965).

(13) A. M. Goodman, Phys. Rev. 152, 785 (1966).

(14) A. M. Goodman, J. Appl. Phys. 37, 3580 (1966).

(15) E. H. Nicollian, A. Goetzberger, and C. N. Berglund, Appl. Phys. Lett. 15, 174 (1969).

(16) E. H. Nicollian and C. N. Berglund, J. Appl. Phys. 41, 3052 (1970).

(17) K. Nagai, Y. Hayashi, and Y. Tarui, Jap. J. Appl. Phys. 14, 1539 (1975).

(18) J. F. Verwey, J. Appl. Phys. 44, 2681 (1973).

(19) T. H. Ning and H. N. Yu, J. Appl. Phys. 45, 5373 (1974).

(20) D. R. Young, J. Appl. Phys. 47, 2098 (1976).

(21) R. Williams and M. H. Woods, J. Appl. Phys. 44, 1026 (1973).

(22) E. Harari, S. Wang, and B. S. H. Royce, J. Appl. Phys. 46, 1310 (1975).

(23) R. C. Hughes, Appl. Phys. Lett. 26, 436 (1975).

(24) J. M. Aitken and D. R. Young, J. Appl. Phys. 47, 1196 (1976).

(25) J. L. Peel and R. C. Eden, IEEE Trans. Nucl. Sci. NS-18, 84 (1971).

(26) R. J. Powell and G. F. Derbenwick, IEEE Trans. Nucl. Sci. NS-18, 99 (1971).

(27) Z. A. Weinberg, Appl. Phys. Lett. 27, 437 (1975).

(28) R. J. Powell, J. Appl. Phys. 46, 4557 (1975).

(29) A. G. Thomas, S. R. Butler, J. I. Goldstein, and P. D. Parry, IEEE Trans. Nucl. Sci. NS-21, 14 (1974).

(30) R. A. Gdula, Tech. Digest, IEEE International Electron Device Meeting, p. 148 (1977).

(31) T. H. Ning, J. Appl. Phys. 49, 4077 (1978).

(32) R. A. Gdula, J. Electrochem. Soc. 123, 42 (1976).

(33) D. J. Coe, Solid-State Electron Dev. 2, 57 (1978).

(34) K. G. Aubuchon, IEEE Trans. Nucl. Sci. NS-18, 117 (1971).

(35) J. M. Aitken and D. R. Young, IEEE Trans. Nucl. Sci. NS-24, 2128 (1977).

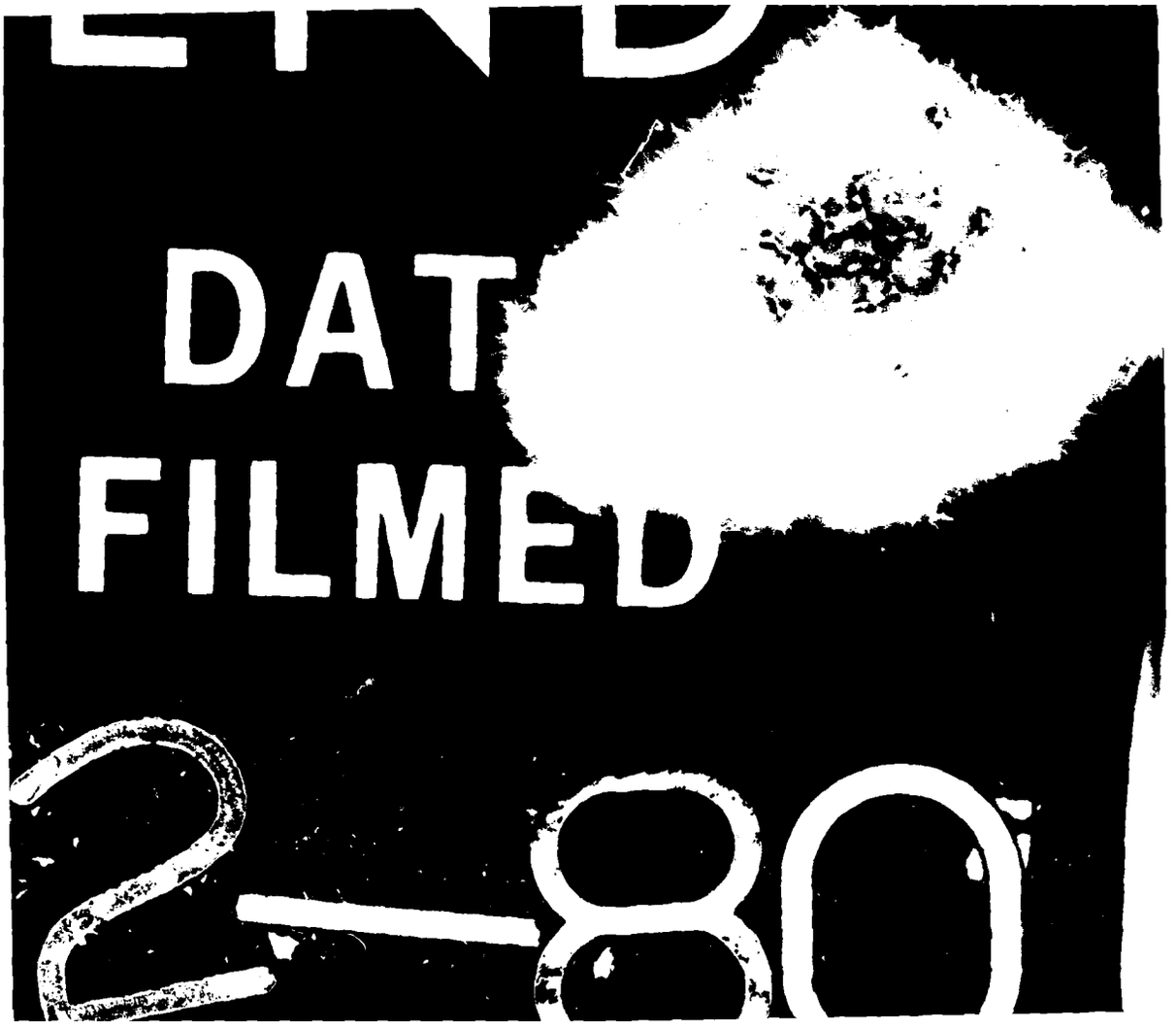
(36) D. R. Young, E. A. Irene, D. J. DiMaria, R. F. DeKeersmaecker, and H. Z. Massoud, J. Appl. Phys. 50, 6366 (1979).

(37) D. R. Young, private communication.

(38) D. R. Lamb and F. R. Badcock, Int. J. Electron. 24, 11 (1968).

(39) G. W. Hughes, Final Report No. PRRL-77-CR-5, February 1977, Contract No. NOOO14-74-C-0185.

(40) H. L. Hughes, IEEE Trans. Nucl. Sci. NS-22, 2118 (1975).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